What is Claimed is:

1. A memory system comprising:

a host integrated circuit;

a first memory controller having at least one associated memory defining a first address space;

a second memory controller having at least one associated memory defining a second address space;

a parity memory for storing parity information associated with data stored in the memories associated with the first and second memory controllers; and

a controller for the storing data in the parity memory, the controller configured to store parity data associated with data stored in the memory associated with the first memory controller in an interleaved fashion with data stored in the memory associated with the second memory controller.

2. The memory system of claim 1, wherein the memory system is a RAID memory system.

3. The memory system of claim 1, wherein the memory system is a RAID 3 memory system.

4. The memory system of claim 1, wherein the first and second memory controllers are capable of being configured to define the first and second address spaces to be non-overlapping.

5. The memory system of claim 1, wherein an address bit is appended to a plurality of address bits used to store and retrieve parity information in the parity memory, wherein the appended address bit is set to a first value when storing and retrieving parity information associated with the first memory controller and the appended address bit is set to a second value when storing and retrieving parity information associated with the second memory controller.

6. The memory system of claim 1, wherein the memory associated with the first memory controller and the memory associated with the second memory controller are different sizes.

7. The memory system of claim 1, wherein the parity memory is at least as large as the larger of the memory associated with the first memory controller and the memory associated with the second memory controller.

8. The memory system of claim 1, wherein there are two memory busses associated with the first memory controller, two memory busses associated with the second memory controller, and two parity memory busses.

9. A memory system comprising:

first data memory coupled to a first memory controller;

second data memory coupled to a second memory controller;

a parity memory coupled to a parity controller, the parity controller being directly coupled to both the first memory controller and the second memory controller;

parity data control logic configured to store and retrieve parity information associated with data stored in both the first data memory and the second data memory, the parity data control logic configured to interleave within the parity memory parity data associated with data stored in the first data memory with parity data associated with data stored in the second data memory.

10. The memory system of claim 9, wherein the memory system is a RAID memory system.

11. The memory system of claim 9, wherein the first and second memory controllers are capable of being configured to define the first and second address spaces to be non-overlapping.

12. The memory system of claim 9, wherein an address bit is appended to a plurality of address bits used to store and retrieve parity information in the parity memory, wherein the appended address bit is set to a first value when storing and retrieving parity information associated with the first memory controller and the appended address bit is set to a second value when storing and retrieving parity information associated with the second memory controller.

13. The memory system of claim 9, wherein the memory associated with the first memory controller and the memory associated with the second memory controller are different sizes.

14. The memory system of claim 9, wherein the parity memory is at least as large as the larger of the memory associated with the first memory controller and the memory associated with the second memory controller.

15. The memory system of claim 9, wherein there are two memory busses associated with the first memory controller, two memory busses associated with the second memory controller, and two parity memory busses.

16. A method for managing parity information associated with a plurality of memory controllers comprising:

generating first parity information associated with data to be stored in a first data memory coupled to a first memory controller;

generating second parity information associated with data to be stored in a second data memory coupled to a second memory controller;

storing the first and second parity information in a parity memory coupled to a parity controller, the first and second parity information being stored in an interleaved fashion within the parity memory.

17. The method of claim 16, wherein storing the first and second parity information more specifically includes managing an address bit of the parity memory, such that the address bit is in one state with storing parity information generated by the first memory controller and the address bit is in a second state when storing parity information generated by the second memory controller.